Remarks

Claims 1-38 are pending in the application. Claims 1 and 18 have been amended, claims 3, 20 and 38 have been canceled and claims 39 and 40 have been added herein. Support for the amendment and new claims can be found, for example, in original claims 3 and 20 and in Fig. 4A. Favorable reconsideration of the application, as amended, is respectfully requested.

I. REJECTION OF CLAIMS 1-4, 7-10, 12, 13, 17-21, 25-27, 29, 30, 34 AND 38 UNDER 35 USC §102

Claims 1-4, 7-10, 12, 13, 17-21, 25-27, 29, 30, 34 and 38 stand rejected under 35 USC 102(e) as being anticipated by U.S. Patent No. 6,661,053 to *Willer et al.* (hereinafter *Willer*). Claim 38 has been canceled herein and thus the rejection of claim 38 has become moot. Withdrawal of the rejection is respectfully requested for at least the following reasons.

Claim 1 has been amended herein to include the features of original claim 3. Claim 1 now recites a memory cell that includes a semiconductor substrate having at least one trench, a recessed channel region formed in the semiconductor substrate below each trench, and a source region and a drain region formed in the semiconductor substrate on opposing sides of each trench, wherein the bottom of the source and drain regions are at a depth from a surface of the semiconductor substrate of about 40 percent to 60 percent of the depth of the floor of the trench. This ratio is advantageous, for example, in that it provides additional channel length, which reduces short channel effects as the device is scaled down in size.

Willer discloses that the optimal trench depth is in the range of 180 nm to 220 nm for a radius r of 70 nm, and 180 nm to 205 nm for a radius r of 55 nm.[1] In other words, the depth of the source and drain zones relative to the trench depth is 68% to 83% for a radius r of 70 nm, and 73% to 83% for a radius r of 55 nm. The Examiner contends that 68% is about 60%. Applicants respectfully disagree with the Examiner.

As noted above, claim 1 specifies a range of about 40% to 60%. Thus, the range spans a 20% window. The Examiner, in contending that 68% is about 60%, is adding 8% to the upper range specified in claim 1, thus increasing the window to 28%. An 8% increase in the 20% window amounts to a 40% increase in the specified window

[1] Column 5, lines 47-52 of *Willer*

(8% increase / 20% window). Clearly, a 40% increase cannot be "about" the specified range. Sixty-eight percent is not within about 40% to 60%, as recited in claims 1 and 18.

Accordingly withdrawal of the rejection of claim 1 is respectfully requested.

The same arguments presented with respect to claim 1 above also apply to claim 18. Accordingly, withdrawal of the rejection of claim 18 is respectfully requested.

Claims 2, 4, 7-10, 12, 13, 17, 19, 21, 25-27, 29, 30 and 34 directly or indirectly depend from either claim 1 or claim 18 and, therefore, can be distinguished from *Willer* for at least the same reasons.

Accordingly, withdrawal of the rejection of claims 2, 4, 7-10, 12, 13, 17, 19, 21, 25-27, 29, 30 and 34 is respectfully requested.

II. REJECTION OF CLAIMS 5, 6, 11, 14-16, 22-24, 28 AND 31-37 UNDER 35 USC §103

Claims 5, 6, 11, 14-16, 22-24, 28, 31-33, 36 and 37 stand rejected under 35 USC 103(a) as being unpatentable over *Willer* in view of U.S. Patent Publication No. 2002/0024092 to *Palm et al.* (hereinafter *Palm*). Claim 35 is rejected under 35 USC 103(a) as being unpatentable over *Willer* in view of U.S. Patent No. 5,960,271 to *Wollesen et al.* (hereinafter *Wollesen*). Withdrawal of the rejections is respectfully requested for at least the following reasons.

Claims 5, 6, 11, 14-16, 22-24, 28 and 31-37 directly or indirectly depend from either claim 1 or claim 18. As was discussed above, amended claims 1 and 18 are distinguishable over *Willer*.

Palm relates to a memory cell formed in a semiconductor body that is arranged in a trench between a source region and a drain region. The gate electrode is separated from the semiconductor material by a dielectric material.

Wollesen relates to a field effect transistor that includes a trench having V-shaped walls formed in a semiconductor substrate. A gate oxide is grown on the V-shaped walls, and the trench is filled with a gate electrode material.

Neither *Palm* nor *Wollesen* disclose the that bottom of the source and drain regions are at a depth from a surface of the semiconductor substrate of about 40 percent to 60 percent of the depth of the floor of the trench, as recited in claims 1 and 18. Thus, claims 1 and 18 can be distinguished over *Willer*, *Palm* and *Wollesen*.

Since claims 5, 6, 11, 14-16, 22-24, 28 and 31-37 directly or indirectly depend from claim 1 or 18, they can be distinguished from the cited art for at least the same reasons.

Accordingly, withdrawal of the rejection of claims 5, 6, 11, 14-16, 22-24, 28 and 31-37 is respectfully requested.

III. New Claims 39-40

New claims 39 and 40 depend from independent claims 1 and 18, respectively. Claims 39 and 40 each recite the aspect wherein the trench is *substantially rectangular.*

Willer discloses a memory cell that includes a trench having either a rectangular shape or a semicylindrical shape.[2] *Willer,* in discussing the semicylindrical shape trench having a radius r, discloses that when the source and drain zones are 150 nm below the top surface of the semiconductor body, the optimal trench depth is in the range of 180 nm to 220 nm for a radius r of 70 nm, and 180 nm to 205 nm for a radius r of 55 nm.[3] In other words, the depth of the source and drain zones relative to the trench depth is 68% to 83% for a radius r of 70 nm, and 73% to 83% for a radius r of 55 nm. Thus, as the radius of the semicylindrical trench is decreased (i.e., the trench approaches a rectangular shape), the ratio of the depth of the source and drain zones relative to the trench depth increases. More specifically, as the radius r approaches zero (a rectangular trench), the ratio of the depth of the source and drain zones with respect to the trench depth would be equal to or higher than the range provided for the radius r of 55 nm, i.e. at least 73% to 83%. Thus, *Willer* does not disclose a memory cell that includes a substantially rectangular trench and a source and drain region formed on opposing sides of the trench, wherein the bottom of the source region and the bottom of the drain region are at a depth from a surface of the semiconductor substrate of about 40% to 60% of the depth of the floor of the trench.

Accordingly, claims 39 and 40 are believed to be allowable.

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[2] See column 5, lines 25-26, Figs. 1 and 2 of *Willer*

[3] Column 5, lines 47-52 of *Willer*

IV. CONCLUSION

Accordingly, all pending claims are believed to be allowable and the application is believed to be in condition for allowance. A prompt action to such end is earnestly solicited.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

In the event any fee or additional fee is due in connection with the filing of this paper, the Commissioner is authorized to charge those fees to our Deposit Account No. 18-0988 (under the above Docket Number). In the event an extension of time is needed to make the filing of this paper timely and no separate petition is attached, please consider this a petition for the requisite extension and charge the fee to our Deposit Account No. 18-0988 (under the above Docket Number).

Respectfully submitted,

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